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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,588	05/23/2001	Jang-Kun Song	6192.0230.AA	8401

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EXAMINER
QI, ZHI QIANG

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 09/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/862,588	SONG ET AL	
	Examin r	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *13-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. According to Applicant's election and suggestion, the elected species are species (1), claims 1-12, drawn to a first embodiment as Figs.1-2. Especially, embodiments are contained in the claims 13-25 need a different search that the burden exists. Currently, no claims appear to be generic.

2. Claims 13-25 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected claims, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 6.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of U.S. Patent Application No. US 2002/0008798 A1 in view of US 6,275,278 (Ono et al).

Although the conflicting claims are not identical, they are not patentable distinct from each other because the claims 1-25 of U.S. Patent Application No. US 2002/0008798 A1 have a very corresponding limitations claimed in the claims 1-12 of this application, and substantially they have the doctrine of obviousness-type double limitations. Especially, claim 1 claimed limitations of the thin film transistor substrate for a liquid crystal display are covered by the claims 1-2 of the U.S. Patent Application No. US 2002/0008798 A1.

For example, **claim 1 of this application** claimed a thin film transistor substrate for a liquid crystal display comprising:

- an insulating substrate;
- a black matrix formed on said insulating substrate having apertures in areas of pixels and shaped as a net;
- an insulating layer covering said black matrix;
- a gate wiring formed on said insulating layer, said gate wiring including gate lines extended in a first direction across said substrate and gate electrode connected to the gate lines;
- a gate insulating layer formed over said gate wiring;
- a semiconductor layer formed over said gate insulating layer;
- an ohmic contact layer formed over said semiconductor layer;
- a data wiring including source electrodes and drain electrodes formed separated from each other over said ohmic contact layer, and data lines

connected to the source electrodes and crossing the gate lines to define the pixels;

- a protective layer formed over said data wiring;
- pixel electrode electrically connected to the drain electrodes.

The claims 1-2 of U.S. Patent Application No. US 2002/0008798 A1

claimed a liquid crystal display comprising:

- a first insulating substrate;
- a black matrix formed on said first insulating substrate, said black matrix being mesh-shaped with opening at pixel areas;
- an insulating layer formed on and covering both said first substrate and said black matrix;
- a gate line assembly formed on said insulating layer, said gate line assembly comprising gate lines proceeding in a horizontal direction, and gate electrodes connected to the gate lines;
- a gate insulating pattern formed on and covering both said insulating layer and said gate line assembly;
- a semiconductor pattern formed on said gate insulating pattern;
- an ohmic contact layer formed on said semiconductor pattern;
- a data line assembly formed on said ohmic contact layer, said data line assembly comprising a source electrode and a drain electrode separated from each other, and data lines connected to the source electrode while crossing over the gate lines to define the pixel areas;

- a protective layer covering said date line assembly and . . . ;
- a pixel electrode connected to the drain electrode, ...

Therefore, the claim 1 of this application and the claims 1-2 of the U.S. Patent Application No. US 2002/0008798 A1 substantially have the doctrine of obviousness-type double limitations, and they have at least an obviousness-type difference.

Claim 2, the limitation is covered by the claim 4 of the U.S. Patent Application No. US 2002/0008798 A1, such as buffer layers placed at the same plane as said gate line assembly or said data line assembly, the buffer layers being positioned between the neighboring separate portions of the black matrix.

Claim 3, the limitation is the same as the claim 5 of the U.S. Patent Application No. US 2002/0008798 A1, such as the black matrix comprising first portions overlapped with the gate lines, the second portions overlapped with the data lines, the first portions and the second portions of said matrix being separated from each other.

Claim 4, the limitation is covered by the claim 3 of the U.S. Patent Application No. US 2002/0008798 A1, such as the black matrix is separated into plural numbers of portions. The portion of the black matrix is removed would be plural numbers of portions.

Claim 5, the limitation is covered by the claim 6 of the U.S. Patent Application No. US 2002/0008798 A1, such as each pixel electrode has a peripheral portion overlapped said black matrix, and that would be the same meaning of the black matrix is formed overlapping adjacent pixel electrodes.

Claim 6, the pixel electrodes and the black matrix having a certain overlapping width that is common and known in the art, because if the overlapping width was too big, the display aperture ratio would be decreased more, and if the overlapping width was too small, the display contrast would be decreased more. In order to compensate the contrast and the aperture ratio, the skilled in the art would find a proper range for the overlapping width of the pixel electrode and the black matrix, and that would have been at least obvious.

Claim 7, Ono discloses (Fig.1 and col.1, line 57 – col.2, line 56) that the pixel electrodes (ITO1) and the data lines (DL) are spaced apart by a certain distance. If the distance was too big, the display aperture ratio would be decreased. If the distance was too small, the cross talk would be increased. In order to realize a bright display screen and lower cross talk, the skilled in the art would find a proper range for the distance spaced apart between the pixel electrodes and the data lines, and that would have been at least obvious.

Claim 8, the insulating layer contains silicon oxide that is common and known in the art, because the property of the silicon oxide has the insulating characteristic between the electrical conductors, and that is conventional.

Claim 9, Ono discloses (col.4, lines 47-49) that the gate insulator (GI) having thickness of 2000 to 5000 Å (0.2μm – 0.5μm), and that is common and known in the art to have a certain thickness for the insulating layer in order to obtain an ensured insulating property.

Claim 10 and 11, the liquid crystal molecules are aligned vertically to the substrate or the liquid crystal molecules are aligned parallel to the substrate that is common and known in the art to control the alignment of the liquid crystal molecules. Because using vertical alignment would achieve high response speed for the image display, and using parallel alignment would achieve wide viewing angle for the image display. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to use vertical alignment or parallel alignment for obtaining a fast response or widen viewing angle.

Claim 12, Ono discloses (Col.6, lines 2-25; Fig.1) that a storage capacity is formed in a region where a pixel electrode (ITO1) overlapping on the gate lines (GL), and the gate insulator (GI) and the protective insulating film (PSV) interposed therebetween. Such storage capacitance would reduce the discharge of charges in the capacity of the liquid crystal and decay in its voltage when the TFT is in the OFF state, such that increases the aperture ratio of the pixel electrode. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to form the overlapping storage capacitance as claimed in claim 12 for obtaining a high aperture ratio of the pixel electrode.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (703) 308-6213.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mike Qi
July 29, 2003

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800